REMARKS

Claim Rejections – 35 U.S.C. §102(b) and §103(a)

The Examiner has rejected base claims 1-49 under 35 U.S.C. 102(b) and 35 U.S.C 103(a) as being anticipated by Tsumura et al and rendered obvious by additional references Luo et al and Fujii et al. It is Applicant's understanding that Tsumura et al, Luo et al, and Fujii et al fail to teach or render obvious the invention specified in claims 1-49.

Claims 1-37

Applicant claims in claims 1-37 a method of coupling a semiconductor die with a next level package. The method includes "providing at least one interconnect and arranging the semiconductor die, the next level package, and the at least one interconnect such that the at least one interconnect is disposed so as to be capable of joining the semiconductor die to the next level package." The method further comprises "generating an electromagnetic flux with an inductor and *exposing the semiconductor die to the electromagnetic flux to preferentially induce eddy currents in the semiconductor die"* (claims 1-16, 34-35) or *"exposing the at least one interconnect to the electromagnetic flux to preferentially induce eddy currents in the interconnect"* (claims 17-33, 36-37) to couple the semiconductor die with the next level package. That is, Applicant claims a method of coupling a semiconductor die with a next level package comprising preferentially inducing eddy currents in the semiconductor die or the at least one interconnect to couple the semiconductor die with a next level package as claimed in claims 1-37 respectively.

It is Applicant's understanding that Tsumura et al fails to disclose a method of coupling a semiconductor die with a next level package comprising preferentially inducing eddy currents in a semiconductor die or interconnect as claimed by Applicant to heat the semiconductor die and couple the semiconductor die with a next level package. Furthermore, Applicants are able to preferentially induce eddy currents by modulating the frequency of the alternating current with respect to the resistivity and magnetic

permeability of each package component. Essentially, Applicant claims a method of exposing a semiconductor die, at least one interconnect, and a next level package to an electromagnetic flux simultaneously such that each may be induced with eddy currents and heated to different temperatures or not induced with eddy currents at all. Tsumura et al does disclose a method of coupling a semiconductor die with a next level package but does not disclose *preferentially* inducing eddy currents in a semiconductor die or an interconnect. Instead, Tsumura et al discloses in Figs 10 and 11 providing the at least one interconnect 21C, arranging the semiconductor die 210A, the next level package 2, and the at least one interconnect 21C such that the at least one interconnect 21C is disposed so as to be capable of joining the semiconductor die 210A to the next level package 2. Tsumura et al further discloses in Figs 3A and 3B generating an electromagnetic flux with an inductor 41A, 41B, and inducing eddy currents in the semiconductor die 210A, the at least one interconnect 21C, and next level package 2. As stated by the Examiner, "the flux is not isolated to just the interconnects, but rather radiates outward from the inductor to produce eddy currents and hence heat in all material within a range including the semiconductor." It is Applicant's understanding that inducing eddy currents in semiconductor die 210A, the at least one interconnect 21C, and next level package 2 is not equivalent to *preferentially* inducing eddy currents in semiconductor die 210A or the at least one interconnect to couple the semiconductor die with the next level package.

Additionally, it is Applicant's understanding that neither of the secondary references, Luo et al nor Fujii et al, discloses a method of coupling a semiconductor die with a next level package by *preferentially* inducing eddy currents in a semiconductor die or *preferentially* inducing eddy currents in the at least one interconnect. Luo et al does disclose a pancake shaped inductor, which can operate in a frequency between 1 to 27 MHz. However, Luo et al fails to disclose a method of coupling a semiconductor die with a next level package by preferentially inducing eddy currents in a semiconductor die or preferentially inducing eddy currents in the at least one interconnect. Fujii et al discloses a flexible substrate but fails to disclose a method of coupling a semiconductor die with a next level package by preferentially inducing eddy currents in a semiconductor die or the at least one interconnect. As such, since neither Tsumura et al, Luo et al, nor Fujii et al, teach a method of coupling a semiconductor die with a next level package by

preferentially inducing eddy currents in a semiconductor die or preferentially inducing eddy currents in the at least one interconnect, the combination of references can not teach or render obvious Applicant's invention as claimed in claims 1-37.

Claims 38-40, 44-46

Applicant claims in claims 38-40 and claims 44-46 a method of coupling a semiconductor die with a next level package. The method includes "providing at least one interconnect and arranging the semiconductor die, the next level package, and the at least one interconnect such that the at least one interconnect is disposed so as to be capable of joining the semiconductor die to the next level package." In claims 38-40, 44-36 the method further comprises "generating an electromagnetic flux with a *pancake coil* to couple the semiconductor die with the next level package." That is, Applicant claims a method of coupling a semiconductor die with a next level package comprising generating an electromagnetic flux with a pancake coil to couple the semiconductor die with a next level package as claimed in claims 38-40 and 44-46 respectively.

It is Applicant's understanding that Tsumura et al does disclose a method of coupling a semiconductor die with a next level package but does not disclose generating an electromagnetic flux with a pancake coil to induce eddy currents in a semiconductor die or an interconnect. It is the Examiner's position that Luo et al's disclosure of a pancake coil used in combination with Tsumura et al's disclosure of a method of coupling a semiconductor die with a next level package by generating an electromagnetic flux with a conventional inductor would be obvious to one skill in the art. However, Applicant strongly disagrees that one skilled in the art would use a plasma enhanced inductor system to couple a semiconductor die with a next level package by generating an electromagnetic flux with a pancake coil to induce eddy currents in a semiconductor die or interconnect.

Furthermore, it is Applicant's understanding that Luo et al's disclosure is non-analogous art to that of Applicant's invention. It is Applicant's understanding that the pancake shaped inductor disclosed by Luo et al is related to a system and method for plasma enhanced processing of semiconductor wafers as opposed to induction based heating for chip attachment as claimed by Applicant. It is Applicant's understanding that

Fujii et al discloses a flexible substrate but fails to disclose a method of coupling a semiconductor die with a next level package by generating an electromagnetic flux with a pancake coil.

As such, since neither Tsumura et al, Luo et al, nor Fujii et al, teach a method of coupling a semiconductor die with a next level package by generating an electromagnetic flux with a pancake coil, the combination of references can not teach or render obvious Applicant's invention as claimed in claims 38-40 and 44-46.

Claims 41-43, 47-49

Applicant claims in claims 41-43 and claims 47-49 a method of coupling a semiconductor die with a next level package. The method includes "providing at least one interconnect and arranging the semiconductor die, the next level package, and the at least one interconnect such that the at least one interconnect is disposed so as to be capable of joining the semiconductor die to the next level package." In claim 41-43 and 47-49, the method further comprises "scanning the inductor around the semiconductor die while generating an electromagnetic flux... to couple the semiconductor die with the next level package." That is, Applicant claims a method of coupling a semiconductor die with a next level package comprising scanning the inductor around the semiconductor die while generating an electromagnetic flux as claimed in claims 41-43 and 47-49 respectively.

It is Applicant's understanding that Tsumura et al does disclose a method of coupling a semiconductor die with a next level package but does not disclose scanning an inductor around a semiconductor die to induce eddy currents in a semiconductor die or an interconnect. Instead, Tsumura et al discloses moving induction heating coil 41 horizontally on wafer chamber lid 171. It is Applicant's understanding that moving an induction heating coil horizontally is not equivalent to scanning an inductor around a semiconductor die to induce eddy currents in a semiconductor die or an interconnect.

Additionally, it is Applicant's understanding that neither of the secondary references, Luo et al nor Fujii et al, discloses a method of coupling a semiconductor die with a next level package by scanning inductor around a semiconductor die while generating an electromagnetic flux. It is also Applicant's understanding that Luo et al's

disclosure of a pancake shaped inductor is fixed in placed in the inductively coupled plasma reactor system (Figure 1, inductor 124) and thus not able to scan around the semiconductor die while generating an electromagnetic flux as claimed by Applicant. It is Applicant's understanding that Fujii et al discloses a flexible substrate, but fails to disclose a method of coupling a semiconductor die with a next level package by scanning an inductor around a semiconductor die while generating an electromagnetic flux.

As such, since neither Tsumura et al, Luo et al, nor Fujii et al, teach a method of coupling a semiconductor die with a next level package by generating an electromagnetic flux to induce eddy currents in a semiconductor die or induce eddy currents in the at least one interconnect the combination of references can not teach or render obvious Applicant's invention as claimed in claims 41-43 and 47-49.

Respectfully submitted,

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